## WHAT IS CLAIMED IS:

1. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

2. The method of claim 1, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

3. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

4. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

5. The method of claim 1, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

6. The method of claim 1, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

7. The method of claim 1, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

8. The method of claim 1, wherein dopants are introduced into the channel region.

9. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

10. The method of claim 9, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

11. The method of claim 9, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

12. The method of claim 9, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

13. The method of claim 9, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

14. The method of claim 9, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

15. The method of claim 9, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

16. The method of claim 9, wherein dopants are introduced into the channel region.

17. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

18. The method of claim 17, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

19. The method of claim 17, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

20. The method of claim 17, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

21. The method of claim 17, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

22. The method of claim 17, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

23. The method of claim 17, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

24. The method of claim 17, wherein dopants are introduced into the channel region.

25. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

26. The method of claim 25, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

27. The method of claim 25, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

28. The method of claim 25, further comprising removing metal not reacted during the reacting process.

29. The method of claim 25, wherein the reacting comprises thermal annealing.

30. The method of claim 25, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

31. The method of claim 25, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

32. The method of claim 25, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

33. The method of claim 25, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

34. The method of claim 25, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

35. The method of claim 25, wherein dopants are introduced into the channel region.

36. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

37. The method of claim 36, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

38. The method of claim 36, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

39. The method of claim 36, further comprising removing metal not reacted during the reacting process.

40. The method of claim 36, wherein the reacting comprises thermal annealing.

41. The method of claim 36, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

42. The method of claim 36, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

43. The method of claim 36, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

44. The method of claim 36, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

45. The method of claim 36, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

46. The method of claim 36, wherein dopants are introduced into the channel region.

47. A method for manufacture of a MOSFET device, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

48. The method of claim 47, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.

49. The method of claim 47, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

50. The method of claim 47, further comprising removing metal not reacted during the reacting process.

51. The method of claim 47, wherein the reacting comprises thermal annealing.

52. The method of claim 47, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

53. The method of claim 47, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

54. The method of claim 47, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

55. The method of claim 47, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

56. The method of claim 47, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

57. The method of claim 47, wherein dopants are introduced into the channel region.

58. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

59. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

60. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

61. The method of claim 58, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

62. The method of claim 58, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

63. The method of claim 58, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

64. The method of claim 58, wherein dopants are introduced into the channel region.

65. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

66. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

67. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

68. The method of claim 65, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

69. The method of claim 65, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

70. The method of claim 65, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

71. The method of claim 65, wherein dopants are introduced into the channel region.

72. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;

providing for a gate electrode in contact with at least a portion of the insulating layer; and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

73. The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

74. The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

75. The method of claim 72, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

76. The method of claim 72, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

77. The method of claim 72, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

78. The method of claim 72, wherein dopants are introduced into the channel region.

79. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

80. The method of claim 79, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

81. The method of claim 79, further comprising removing metal not reacted during the reacting process.

82. The method of claim 79, wherein the reacting comprises thermal annealing.

83. The method of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

84. The method of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

85. The method of claim 79, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

86. The method of claim 79, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

87. The method of claim 79, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

88. The method of claim 79, wherein dopants are introduced into the channel region.

89. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

90. The method of claim 89, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

91. The method of claim 89, further comprising removing metal not reacted during the reacting process.

92. The method of claim 89, wherein the reacting comprises thermal annealing.

93. The method of claim 89, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

94. The method of claim 89, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

95. The method of claim 89, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

96. The method of claim 89, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

97. The method of claim 89, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

98. The method of claim 89, wherein dopants are introduced into the channel region.

99. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

100. The method of claim 99, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

101. The method of claim 99, further comprising removing metal not reacted during the reacting process.

102. The method of claim 99, wherein the reacting comprises thermal annealing.

103. The method of claim 99, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

104. The method of claim 99, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

105. The method of claim 99, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

106. The method of claim 99, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

107. The method of claim 99, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

108. The method of claim 99, wherein dopants are introduced into the channel region.